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124

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/998,834	11/15/2001	Craig Nemecek	CYPR-CD01221M	7168

7590 09/20/2004

WAGNER, MURABITO & HAO LLP
Third Floor
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EXAMINER	
NGUYEN BA, HOANG VU A	

ART UNIT	PAPER NUMBER
2122	

DATE MAILED: 09/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/998,834	NEMECEK, CRAIG	
	Examiner	Art Unit	
	Hoang-Vu A Nguyen-Ba	2122	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) ____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 November 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the application filed November 15, 2001.

2. The priority date considered for this application is November 15, 2001.

3. Claims 1-21 have been examined.

Drawings

4. This application has been filed with informal drawings, which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

Specification

5. The specification is objected to because of the following minor informalities:

a. In the Abstract: the verb "performs" at line 10 should be – perform –. The same typographical error should also be corrected in line 3, page 6 of the Specification.

b. In the Specification: the term "born" should be changed to – borne – in line 8 of page 9.

Claim Objections

6. Claims 2 and 13 are objected to because of the following informality:

In claims 2 and 13, the term "POD" should be spelled out the first time it is used. Since, it is not known what POD stands for, the Office interprets POD to mean – a target board – as illustrated as item 24 in Figure 1 of U.S. Patent 5,590,354 to Klapproth et al. ("Klapproth").

Appropriate correction is required.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. § 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 5, 6, 8, 16, 17, 20, 21 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 5, 6, 16, 17, 20 and 21:

Claims 5, 6, 16, 17, 20 and 21 are indefinite because these claims and the specification do not provide information about the lowest and highest limits of the frequency at which the microcontroller is operating. An ordinary skilled person in the art would not be reasonably apprised of the scope of the invention.

Claim 8:

Claim 8 recites "a first memory of an ICE" and a "second memory of a microcontroller." The claim is unclear because it is not certain whether or not the ICE and the microcontroller both have more than one memory and the first memory of a plurality of memories of an ICE and the second memory of a plurality of memories of the microcontroller are initialized. Furthermore, the claim is indefinite because it is not known how many memories the ICE and microcontroller do possess.

Claim Rejections – 35 USC § 103

9. The following is a quotation of the 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1-7 and 18-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art (APA) in Figure 1 and pages 1-4 of Applicant's background of the invention in view of U.S. Patent No. 5,590,354 to Klapproth et al.

Claim 1

APA disclose at least:

a computer system for controlling a debugging process (see at least Figure 1);

an ICE coupled to the computer system, wherein the ICE emulates the microcontroller, and wherein the ICE is configured to run the microcontroller code cooperatively with the microcontroller to implement the debugging process (see at least Figure 1, item 100 and related discussion in the specification). APA does not specifically disclose:

a microcontroller installed on a test circuit, the microcontroller configured to run microcontroller code and

a debug interface included in the microcontroller for communicatively

coupling the microcontroller and the ICE, the interface configured to enable data transmission when the microcontroller is operating at a reduced speed and to disable data transmission when the microcontroller is operating at a normal speed.

However, in an analogous art, Klapproth teaches a microcontroller provided with hardware for supporting debugging as based on boundary scan standard-type extensions having the claimed debug interface (see Figure 1, item 46 and related discussion in the specification) and the claimed microcontroller (see Figure 1, item 20 and related discussion in the specification).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine Klapproth with APA because this combination would reduce the cost and time of debugging and manufacturing microcontrollers.

Claim 18

Since claim 18 recites the same features of claim 1, the same rejection is thus applied.

Claim 2

The rejection of base claim 1 is incorporated. APA does not specifically disclose *wherein the test circuit is a POD.* However, Klaproth teaches a target board on which a microcontroller can be attached for the test operation. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine Klapproth with APA because this combination would reduce the cost and time of debugging and manufacturing microcontrollers.

Claim 3

The rejection of base claim 1 is incorporated. APA further discloses *wherein the ICE includes a field programmable gate array (FPGA) where the microcontroller is emulated* (see at least Figure 1, item 130 and related discussion in the specification).

Claims 4 and 19

Rejections of base claims 1 and 18 are incorporated. APA does not specifically disclose *wherein the debug interface performs I/O operations with the ICE for the microcontroller.*

However, Klapproth teaches a JTAG interface (see at least Figure 1, item 46 and related discussion in the specification) of a standard microcontroller that can communicate with that of the host (see at least Figure 1, item 30 and related discussion in the specification) for the purpose of making test of microcontroller more efficient. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine Klapproth with APA because this combination would reduce the cost and time of debugging and manufacturing microcontrollers.

Claims 5 and 20

Rejections of base claims 1 and 18 are incorporated. APA does not specifically disclose *wherein the low speed is 3 Mhz or lower.* However, Klapproth teaches that test and system clocks could be synchronized (see at least 4:47-57).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Klapproth so that operating speed of microcontroller could be set by a user because this would help improve the debugging process.

Claims 6 and 21

Rejections of base claims 1 and 18 are incorporated. APA does not specifically disclose *wherein the normal speed is 24 Mhz or above.* However, Klapproth teaches that test and system clocks could be synchronized (see at least 4:47-57).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Klapproth so that operating speed of microcontroller could be set by a user because this would help improve the debugging process.

Claim 7

The rejection of base claim 1 is incorporated. APA does not specifically disclose *a CAT 5 cable for communicatively coupling the ICE and the debug interface.* However, Klapproth teaches requisite interconnection support equipment (see at least Figure 1, item 34 and related discussion in the specification) between microcontroller and host machine for a trouble-free debug session.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to Klapproth with APA because this combination would reduce the cost and time of debugging and manufacturing microcontrollers.

Allowable Subject Matter(s)

10. Claims 8-17 are allowable.

11. Following is the examiner's reason for allowance:

The prior art of record, taken individually or in combination, fails to teach the combination of the following features of claim 8, features which when taken individually would not be allowable:

a) initializing a first memory of an ICE and a second memory of a microcontroller with microcontroller test code;

b) executing the microcontroller test code on the microcontroller and on the ICE simultaneously;

c) decreasing an operating frequency of the microcontroller from a normal speed to a reduced speed, the decreasing commanded by the ICE during an execution halt;

d) while at the reduced speed, transmitting debugging commands between the ICE and the microcontroller via a debug interface of the microcontroller; and

e) increasing the operating frequency from reduced speed to normal speed after the debugging commands are transmitted.

12. Claims 9-17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoang-Vu A Nguyen-Ba whose telephone number is (703) 305-0103. The examiner can normally be reached on Tuesday-Friday, 6:00 – 16:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Dam can be reached on (703) 305-4552. After October 25, 2004, the examiner can be reached at (571) 272-3701 and the examiner's supervisor at (571) 272-3695. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANTONY NGUYEN-BA
PRIMARY EXAMINER
Art Unit 2122
September 13, 2004